ALPHA & OMEGA
SEMICONDUCTOR, LTD

Green Product

RoHS Compliant

AOD609
Complementary Enhancement Mode Field Effect Transistor

General Description
The AOD609 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.
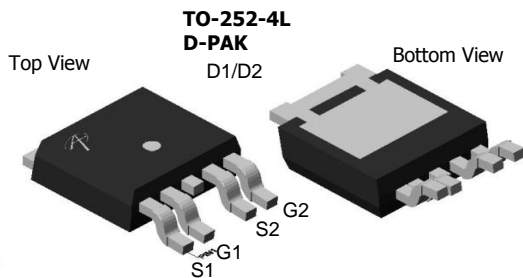
-RoHS Compliant
-Halogen Free*

Features
n-channel
V_{DS} (V) = 40V, I_D = 12A (V_{GS}=10V)
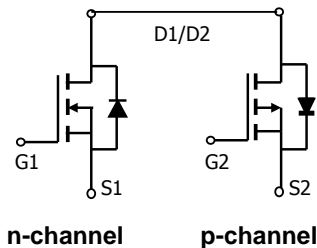$R_{DS(ON)}$< 30mΩ (V_{GS}=10V)
$R_{DS(ON)}$< 40mΩ (V_{GS}=4.5V)
p-channel
V_{DS} (V) = -40V, I_D = -12A (V_{GS}=-10V)
$R_{DS(ON)}$< 45mΩ (VGS= -10V)
$R_{DS(ON)}$< 66mΩ (VGS= -4.5V)
100% UIS Tested!
100% Rg Tested!

TO-252-4L D-PAK

Top View — D1/D2

Bottom View

Top View Drain Connected to Tab

G2, S2, G1, S1

D1/D2, G1, S1, G2, S2

n-channel   **p-channel**

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [B,H]	T_C=25°C	I_D	12	-12	A
	T_C=100°C		12	-12	
Pulsed Drain Current [B]		I_{DM}	30	-30	
Avalanche Current [C]		I_{AR}	14	-20	
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	9.8	20	mJ
Power Dissipation	T_C=25°C	P_D	27	30	W
	T_C=100°C		14	15	
Power Dissipation	T_A=25°C	P_{DSM}	2	2	W
	T_A=70°C		1.3	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	-55 to 175	°C

Thermal Characteristics: n-channel and p-channel

Parameter		Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient [A,D]	t ≤ 10s	$R_{θJA}$	n-ch	17.4	25	°C/W
Maximum Junction-to-Ambient [A,D]	Steady-State		n-ch	50	60	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{θJC}$	n-ch	4	5.5	°C/W
Maximum Junction-to-Ambient [A,D]	t ≤ 10s	$R_{θJA}$	p-ch	16.7	25	°C/W
Maximum Junction-to-Ambient [A,D]	Steady-State		p-ch	50	60	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{θJC}$	p-ch	3.5	5	°C/W

N Channel Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V		40			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=40V, V$_{GS}$=0V				1	µA
			T$_J$=55°C			5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±20V				±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$=250µA		1.7	2.5	3	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=10V, V$_{DS}$=5V		30			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=12A			24	30	mΩ
			T$_J$=125°C		37	46	
		V$_{GS}$=4.5V, I$_D$=8A			31	40	
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=12A			25		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V			0.76	1	V
I$_S$	Maximum Body-Diode Continuous Current [H]					12	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=20V, f=1MHz			516	650	pF
C$_{oss}$	Output Capacitance				82		pF
C$_{rss}$	Reverse Transfer Capacitance				43		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz			4.6	6.9	Ω
SWITCHING PARAMETERS							
Q$_g$ (10V)	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=20V, I$_D$=12A			8.3	10.8	nC
Q$_{gs}$	Gate Source Charge				2.3		nC
Q$_{gd}$	Gate Drain Charge				1.6		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=20V, R$_L$=1.4Ω, R$_{GEN}$=3Ω			6.4		ns
t$_r$	Turn-On Rise Time				3.6		ns
t$_{D(off)}$	Turn-Off DelayTime				16.2		ns
t$_f$	Turn-Off Fall Time				6.6		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=12A, dI/dt=100A/µs			18	24	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=12A, dI/dt=100A/µs			10		nC

A: The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25° C. The power dissipation P$_{DSM}$ and current rating I$_{DSM}$ are based on T$_{J(MAX)}$=150° C, using the steady state junction-to-ambient thermal resistance.
B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C: Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=175° C.
D. The R$_{θJA}$ is the sum of the thermal impedence from junction to case R$_{θJC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25° C.
H. The maximum current rating is limited by bond-wires.

P-Channel Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$= -250µA, V$_{GS}$=0V		-40			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$= -40V, V$_{GS}$=0V				-1	µA
			T$_J$=55°C			-5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±20V				±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$= -250µA		-1.7	-2	-3	V
I$_{D(ON)}$	On state drain current	V$_{GS}$= -10V, V$_{DS}$= -5V		-30			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$= -10V, I$_D$= -12A			36	45	mΩ
			T$_J$=125°C		52	65	
		V$_{GS}$= -4.5V, I$_D$= -8A			51	66	
g$_{FS}$	Forward Transconductance	V$_{DS}$= -5V, I$_D$= -12A			22		S
V$_{SD}$	Diode Forward Voltage	I$_S$= -1A,V$_{GS}$=0V			-0.76	-1	V
I$_S$	Maximum Body-Diode Continuous Current [H]					-12	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$= -20V, f=1MHz			900	1125	pF
C$_{oss}$	Output Capacitance				97		pF
C$_{rss}$	Reverse Transfer Capacitance				68		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz			14		Ω
SWITCHING PARAMETERS							
Q$_g$ (-10V)	Total Gate Charge	V$_{GS}$= -10V, V$_{DS}$= -20V, I$_D$= -12A			16.2	21	nC
Q$_g$ (-4.5V)	Total Gate Charge				7.2	9.4	nC
Q$_{gs}$	Gate Source Charge				3.8		nC
Q$_{gd}$	Gate Drain Charge				3.5		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$= -10V, V$_{DS}$= -20V, R$_L$=1.4Ω, R$_{GEN}$=3Ω			6.2		ns
t$_r$	Turn-On Rise Time				8.4		ns
t$_{D(off)}$	Turn-Off DelayTime				44.8		ns
t$_f$	Turn-Off Fall Time				41.2		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$= -12A, dI/dt=100A/µs			21	27	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$= -12A, dI/dt=100A/µs			14		nC

A: The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25°C. The power dissipation P$_{DSM}$ and current rating I$_{DSM}$ are based on T$_{J(MAX)}$=150°C, using t ≤ 10s junction-to-ambient thermal resistance.
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D. The R$_{θJA}$ is the sum of the thermal impedence from junction to case R$_{θJC}$ and case to ambient.
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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL
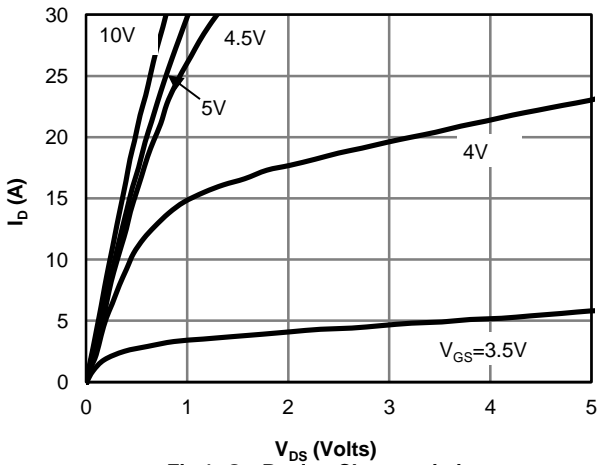

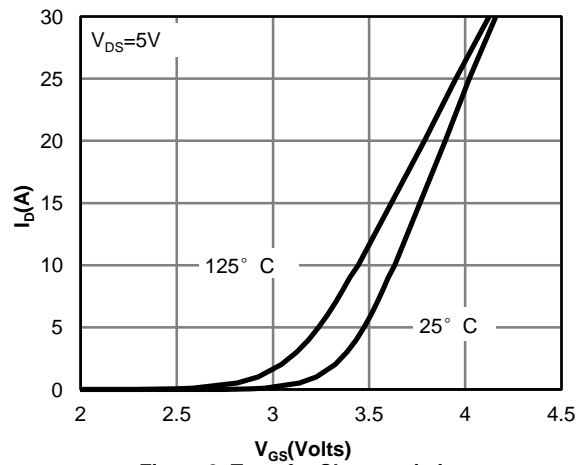**Fig 1: On-Region Characteristics**
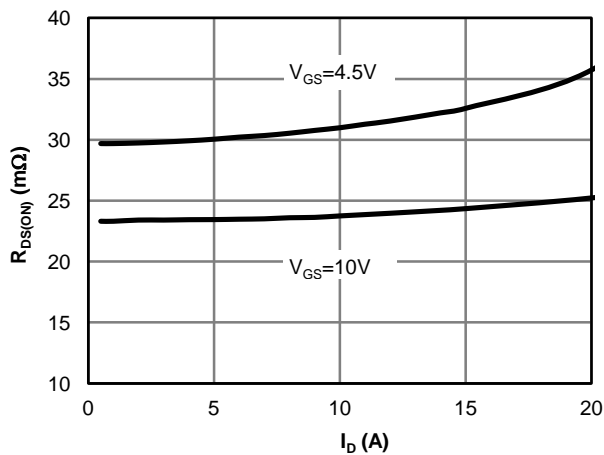

Figure 2: Transfer Characteristics

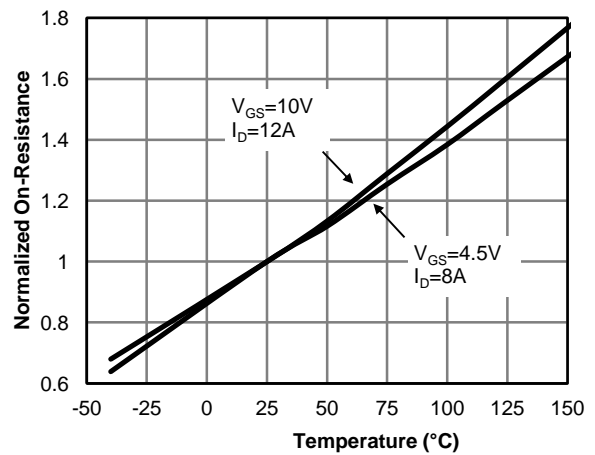**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**

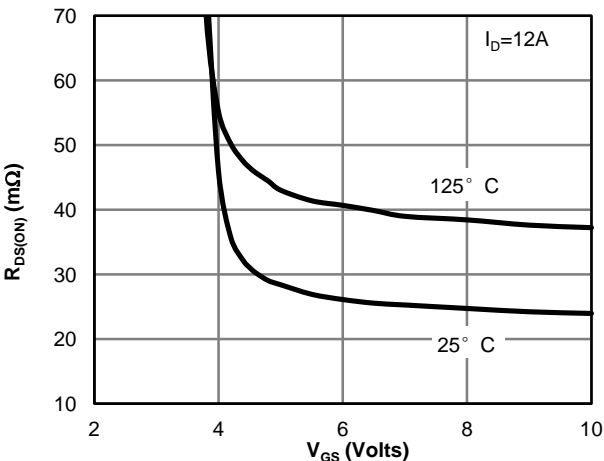**Figure 4: On-Resistance vs. Junction Temperature**
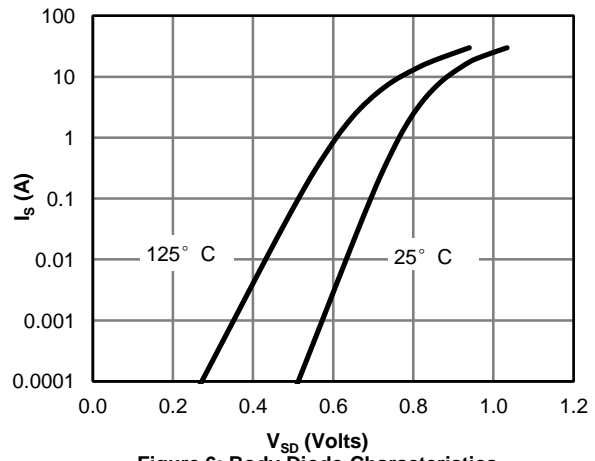

Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics

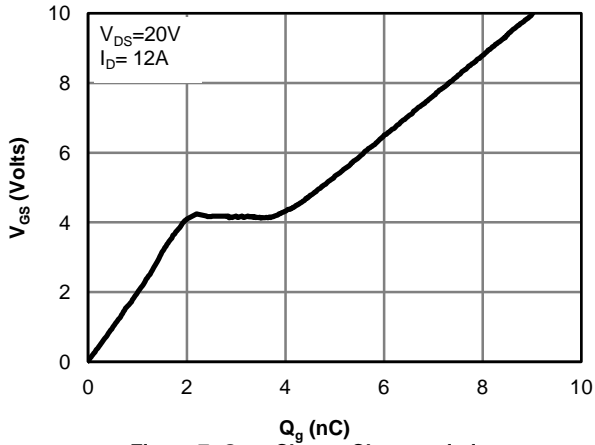**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL**
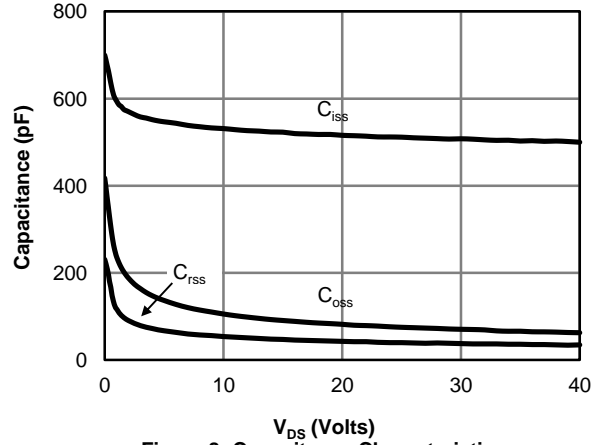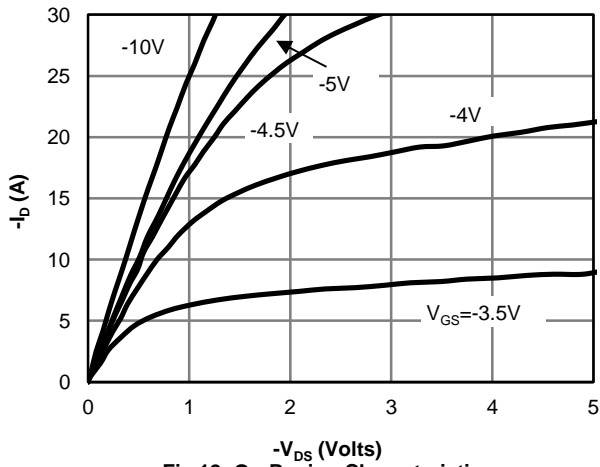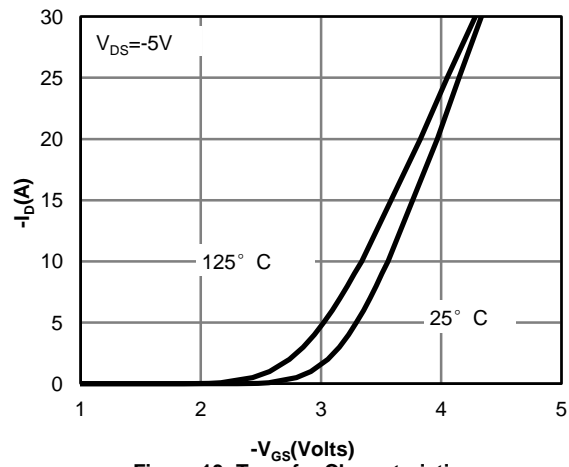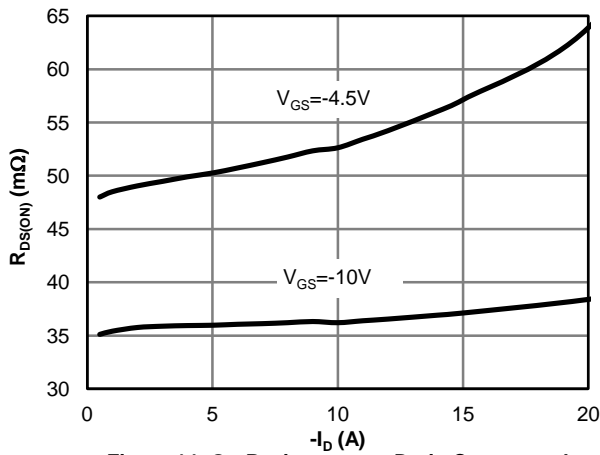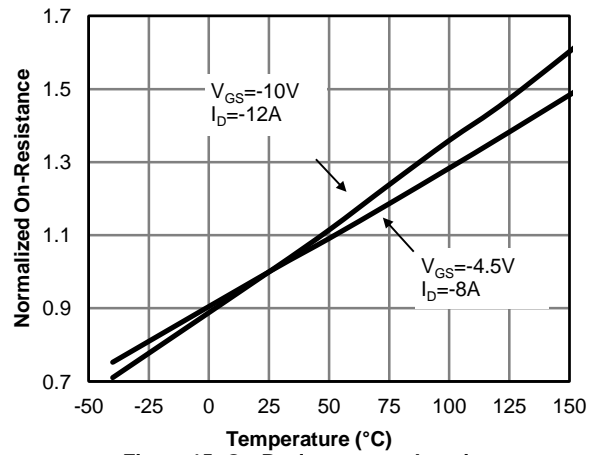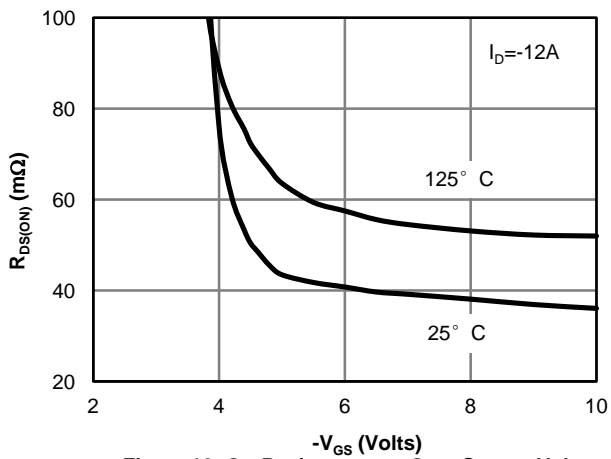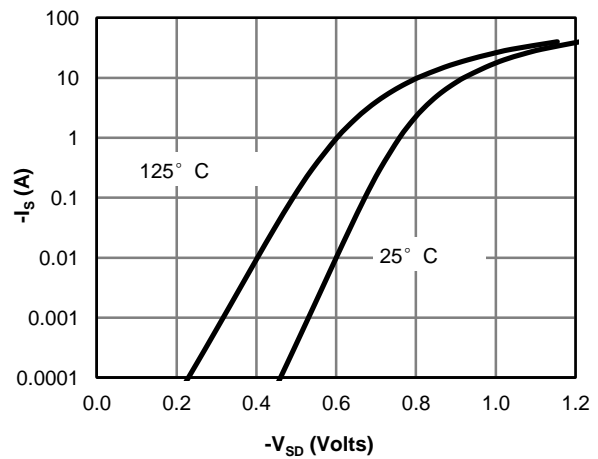

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics
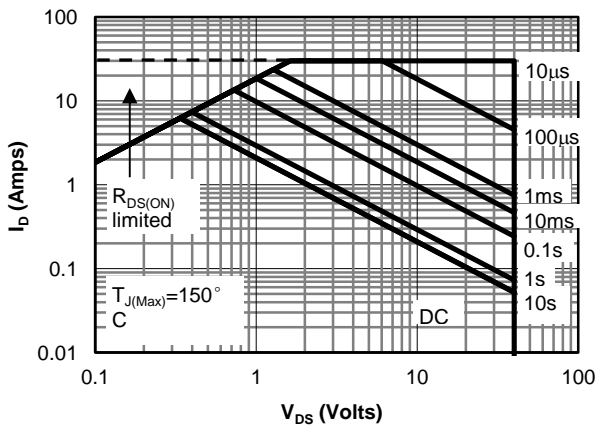
Figure 9: Maximum Forward Biased Safe Operating Area (Note E)
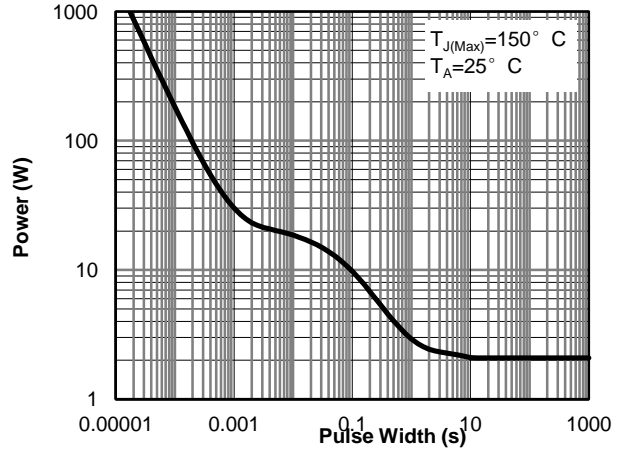
Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)
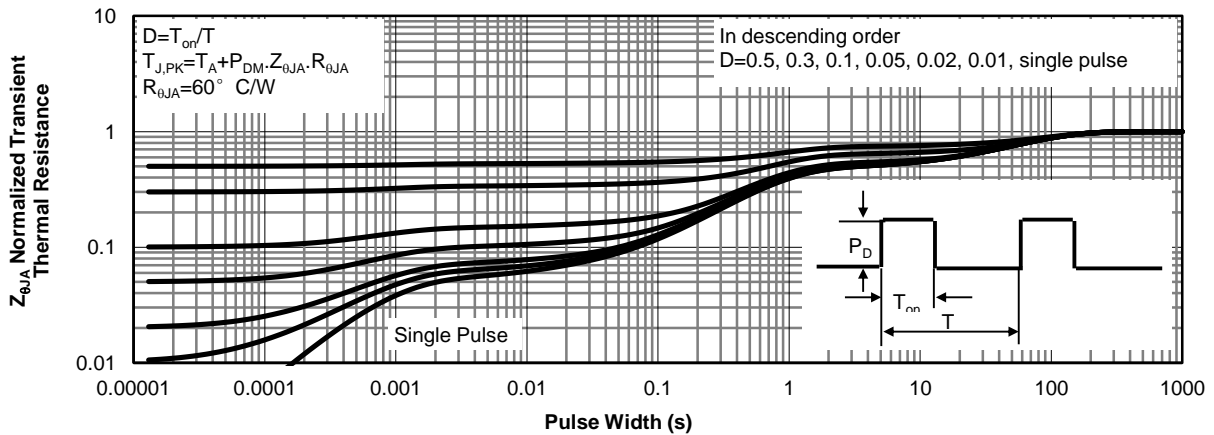
Figure 11: Normalized Maximum Transient Thermal Impedance
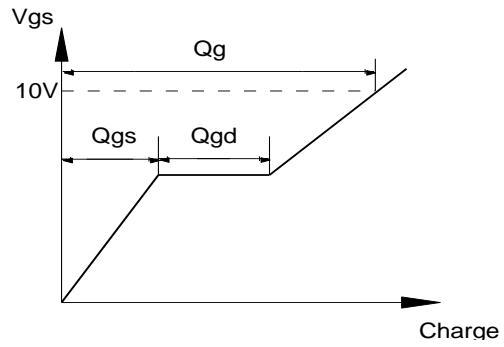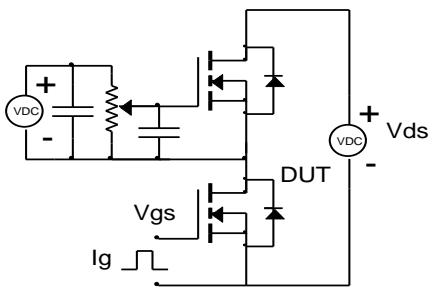
Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2\ LI_{AR}^2$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$
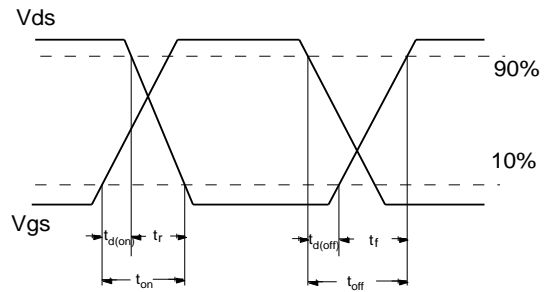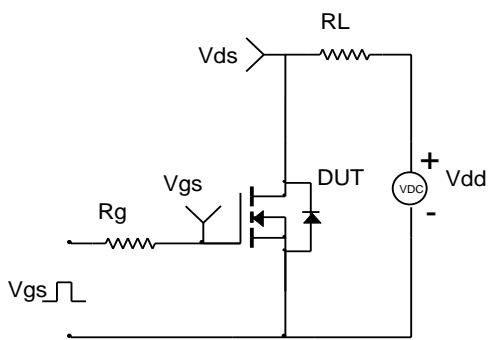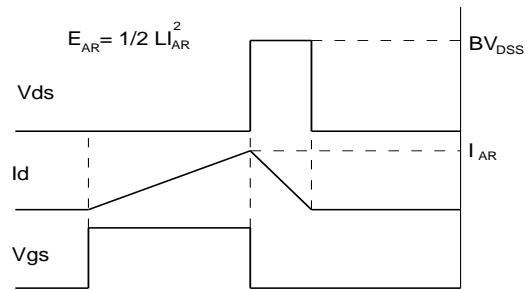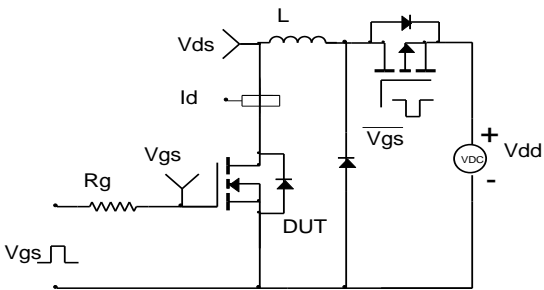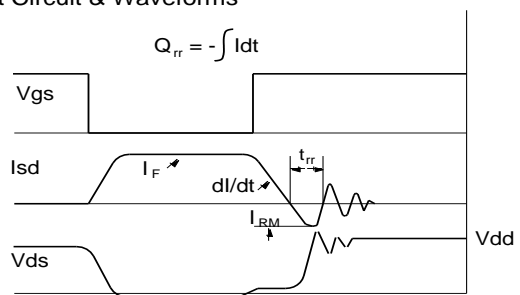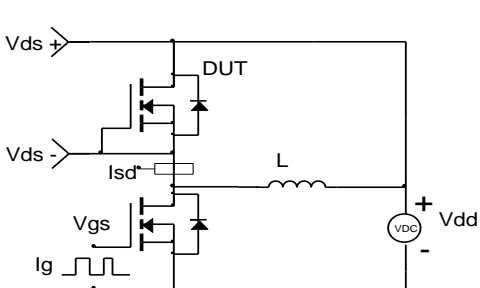
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

Fig 12: On-Region Characteristics

Figure 13: Transfer Characteristics

Figure 14: On-Resistance vs. Drain Current and Gate Voltage

Figure 15: On-Resistance vs. Junction Temperature

Figure 16: On-Resistance vs. Gate-Source Voltage

Figure 17: Body-Diode Characteristics

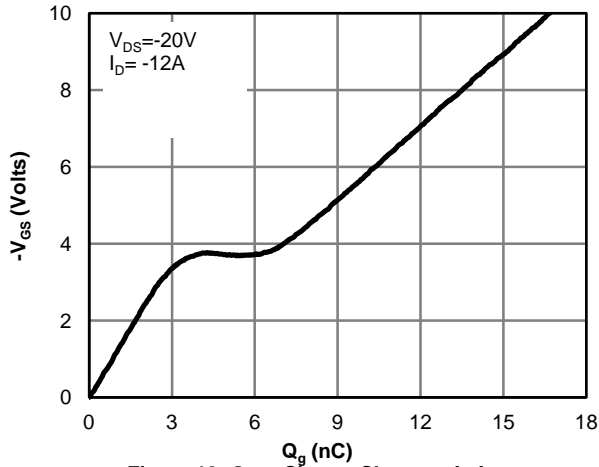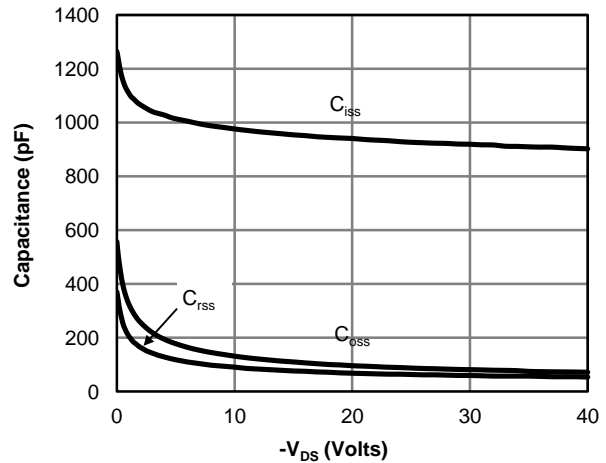**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL**

Figure 18: Gate-Charge Characteristics

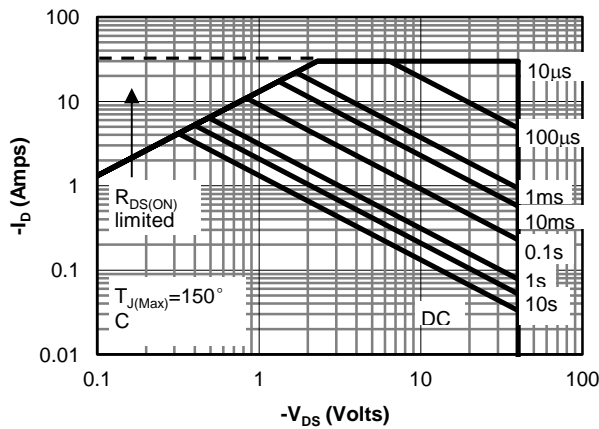**Figure 19: Capacitance Characteristics**

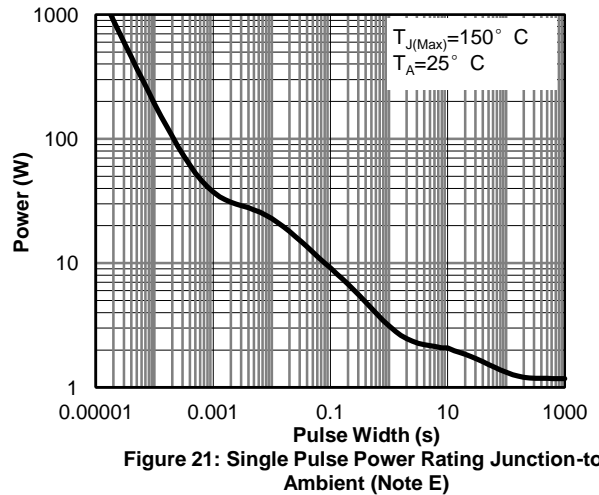**Figure 20: Maximum Forward Biased Safe Operating Area (Note E)**

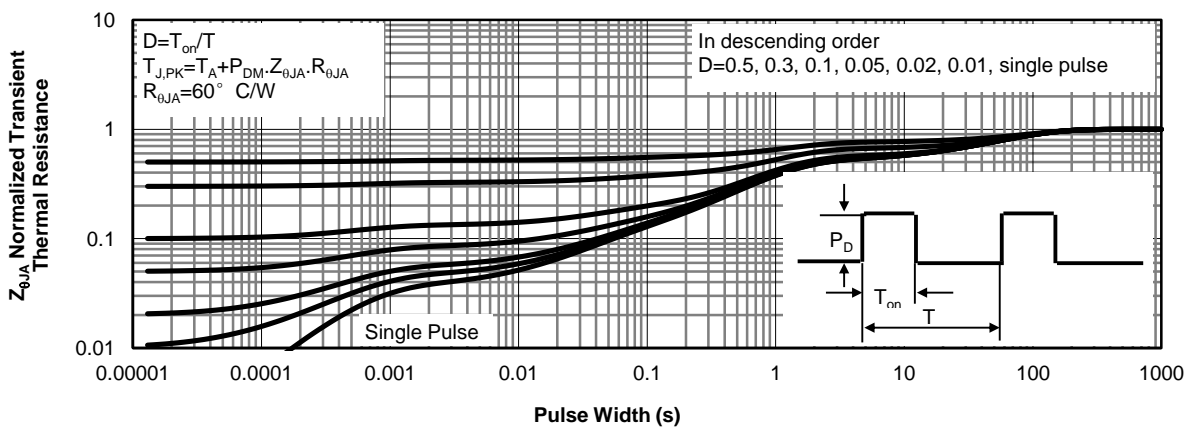**Figure 21: Single Pulse Power Rating Junction-to-Ambient (Note E)**
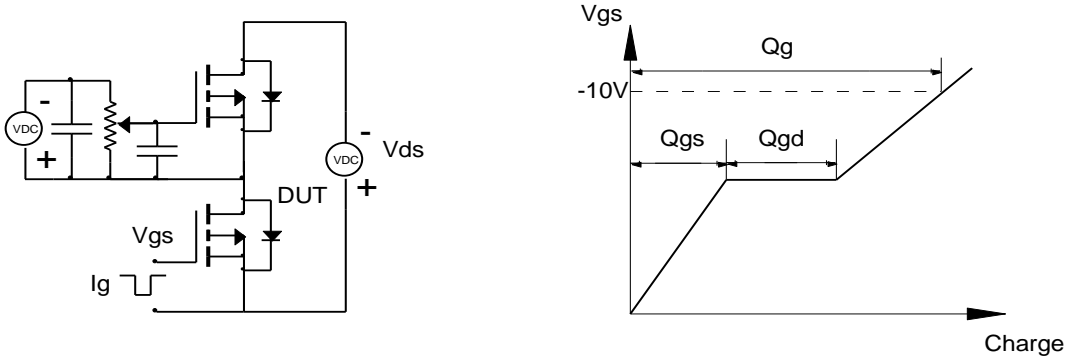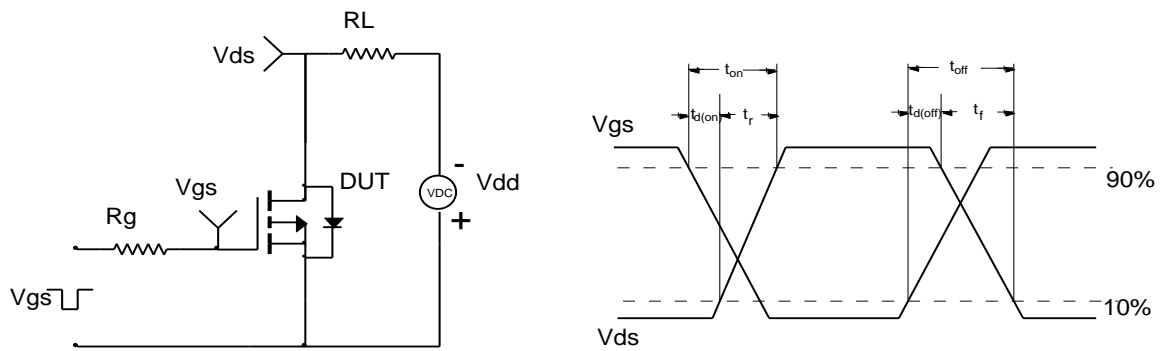

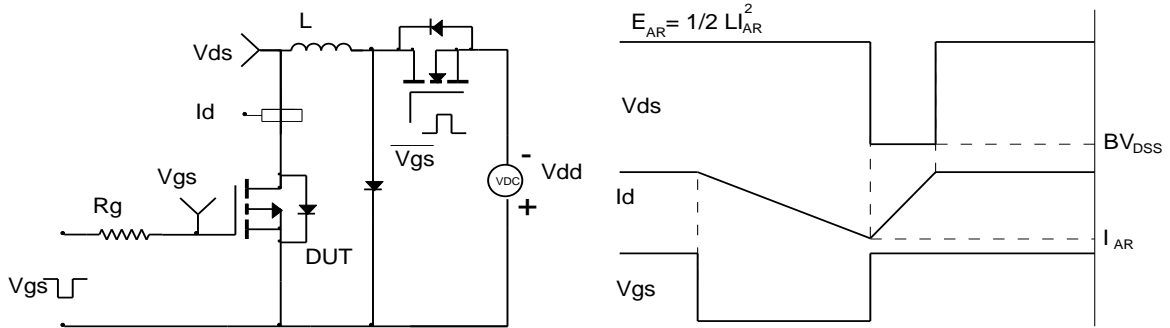**Figure 22: Normalized Maximum Transient Thermal Impedance**

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$E_{AR} = 1/2 \ LI_{AR}^2$

Diode Recovery Test Circuit & Waveforms

$Q_{rr} = -\int I \, dt$
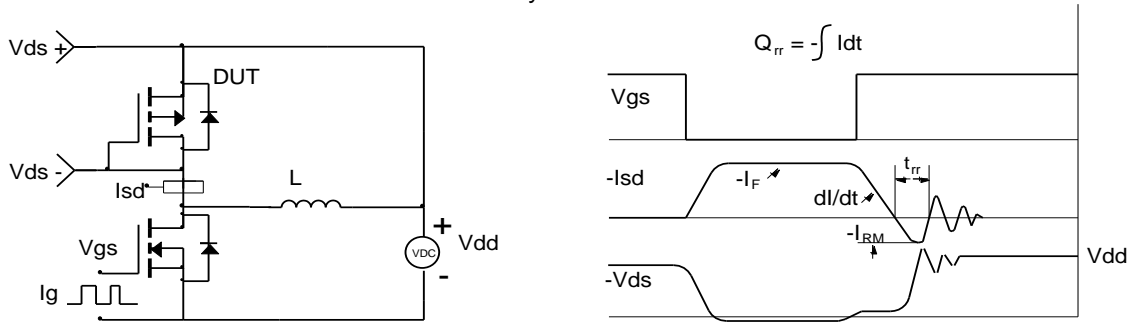
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